

AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 23, line 18:

The third correlator 2c calculates a correlation value between the third quasi-coherent signal SS3 and a spreading code sequence generated by the spreading code generator 3c. The level detector 4c generates a chip synchronous signal CS3 indicative of a received signal phase position having the maximum correlation. The chip synchronous signal CS3 is then used for establishment of the synchronization. When receiving and examining the chip synchronous signal CS3, the third despreading circuit 5c despreads the quasi-coherent signal SS3 to produce a despread signal DS3. The ~~[[first]]~~ third despreading circuit 5c despreads the quasi-coherent signal SS3 using another spreading code sequence (not shown) having a phase indicated by the chip synchronous signal CS3. The third synchronization judging circuit 6c examines the despread signal DS3 to judge the synchronization. More particularly, the third synchronization judging circuit 6c detects the synchronization between the quasi-coherent signal SS3 and the other spreading code sequence. Upon detecting the synchronization, the third synchronization judging circuit 6c informs the third spreading code generator 3c of the synchronization by sending a synchronization informing signal SI3. When receiving the sync informing signal SI3 indicative of the synchronization, the third spreading code generator 3c generates a spreading code sequence of the phase at the timing of the synchronization. The phase of the spreading code sequence is then fixed. As the phase of the spreading code sequence generated by the third diffusion generator circuit 3c is fixed, the synchronization can be maintained.